IN THE CLAIMS

This listing of the claim will replace all prior versions and listings of claim in the present application.

Listing of Claims

1. (currently amended)An automatic equalization circuit for receiving a digital training signal and a digital data signal and outputting a digital data signal equalized, comprising;

a first automatic equalization unit including a first equalizer, to which said digital training signal and a digital data signal are applied, for equalizing said digital data signal;

a memory for storing said digital training signal;

a second automatic equalization unit coupled with said memory, for outputting an updating signal therefrom, said second automatic equalization unit comprising a second equalizer for outputting said updating signal, a training signal generator for outputting an either one of an in-phase component and a quadrature component signals of a training signal, the other one of which is zero, and a tap coefficient calculating unit coupled with said second equalizer, for outputting a tap coefficient value in comparison with said digital training signal from said memory and an output from said training signal generator and updating the tap coefficient of said second equalizer; and

a phase rotator for rotating a phase of either one of an input signal and an output signal of said first automatic equalization unit, said digital training signal

supplied to said memory and said updating signal outputted from said second equalizer;

wherein said updating signal from said second equalizer is supplied to said first equalizer, so that a equalization characteristic of said first equalizer is updated.

2. (original) An automatic equalization circuit according to claim 1, wherein a structure of said second equalizer has substantially the same structure as said first equalizer.

3. (original) An automatic equalization circuit according to claim 1, wherein, said digital training signal and digital data signal are supplied to said first automatic equalization unit through a delay circuit, the delay time of which is predetermined.

4. (original) An automatic equalization circuit according to claim 1, wherein said first and second equalizer are feedforward type equalizers and further comprising a third equalizer coupled with an output terminal of said first automatic equalization unit and a fourth equalizer coupled with said training signal generator, wherein said third and fourth equalizer are feedback type equalizers and an output from said fourth equalizer is applied to said third equalizer in order to update an equalization characteristic of said third equalizer.

5. (original) An automatic equalization circuit according to claim 1, wherein said phase rotator is coupled between said first equalizer and said second equalizer to rotate the phase of said updating signal from said second equalizer.

6. (original) An automatic equalization circuit according to claim 1, wherein said phase rotator is coupled with said memory, through which said input signal is supplied to said memory, so that the phase of said digital training signal to said memory is rotated.

7. (original) An automatic equalization circuit according to claim 1, wherein said phase rotator is coupled with said first equalizer, through which said digital training signal and said digital data signal are supplied to said first equalizer.

8. (original) An automatic equalization circuit according to claim 1, wherein said phase rotator is coupled with said first equalizer, through which said digital data signal from said first automatic equalization unit is outputted.

9. (original) An automatic equalization circuit according to claim 1, wherein said digital training signal is a signal corresponding to two signal points having an average power substantially equal to an average power of data signals having signal points on a data signal constellation plane.

10. (currently amended)A receiver circuit for reproducing a training signal and a data signal modulated by a digital multilevel modulation system, comprising:

a signal processing unit, to which said training signal and a data signal are supplied, for producing a digital training signal and a digital data signal;

a first automatic equalization unit including a first equalizer coupled with said signal processing unit, for equalizing said digital data signal, and outputting a digital data signal equalized;

a memory coupled with said signal processing unit, for storing said digital training signal;

a second automatic equalization unit coupled with said memory, for outputting an updating signal therefrom, said second automatic equalization unit comprising a second equalizer for outputting said updating signal, a training signal generator for outputting an either one of an in-phase component and a quadrature component signals of a training signal, the other one of which is zero, and a tap coefficient calculating unit coupled with said second equalizer, for outputting a tap coefficient value in comparison with said digital training signal from said memory and an output from said training signal generator and updating the tap coefficient of said second equalizer; and

a phase rotator for rotating a phase of either one of an input signal and an output signal of said first automatic equalization unit, said digital training signal supplied to said memory and said updating signal outputted from said second equalizer.

wherein said updating signal from said second equalizer is supplied to said first equalizer, so that a equalization characteristic of said first equalizer is updated.

11. (original) A receiver circuit according to claim 10, wherein a structure of said second equalizer has substantially the same structure as said first equalizer.

12. (currently amended)A receiver circuit according to claim 10, further comprising:

a delay circuit coupled between said signal processing unit and said first automatic equalization unit, the delay time of which is predetermined.

13. (original) A receiver circuit according to claim 10, wherein said first and second equalizer are feedforward type equalizers and further comprising a third equalizer coupled with an output terminal of said first automatic equalization unit and a fourth equalizer coupled with said training signal generator, wherein said third and fourth equalizers are feedback type equalizers and an output from said fourth equalizer is applied to said third equalizer in order to update an equalization characteristic of said third equalizer.

14. (original) A receiver circuit according to claim 10, wherein said phase rotator is coupled between said first and second equalizers to rotate the phase of said updating signal from said second equalizer.

15. (original) A receiver circuit according to claim 10, wherein said phase rotator is coupled between said signal processing unit and said memory in order to rotate the phase of said digital training signal to said memory.

16. (original) A receiver circuit according to claim 10, wherein said phase rotator is coupled between said signal processing unit and said first automatic equalization unit, and said digital training and data signals from said signal processing unit are supplied to said first automatic equalization unit through said phase rotator.

17. (original) A receiver circuit according to claim 10, wherein said phase rotator is coupled with said first equalizer, through which said digital data signal from said first automatic equalization unit is outputted.

18. (original) A receiver circuit according to claim 10, wherein said digital training signal is a signal corresponding to two signal points having an average power substantially equal to an average power of data signals having signal points on a data signal constellation plane.